Optical Buffering and Time-Slot Interchanger with integrated Si-based delay lines

Miltiadis Moralis-Pegios(1), George Mourgias-Alexandris(1), Nikos Terzenidis(1), Matteo Cherchi(3), Mikko Harjanne(3), Timo Aalto(3), Amalia Miliou(1), Nikos Pleros(1), Kostantinos Vyrso kokinos(2)

(1) Dpt. of Informatics, Aristotle University of Thessaloniki, Thessaloniki Greece
(2) Dpt. of Physics, Aristotle University of Thessaloniki, Thessaloniki Greece
(3) VTT Technical Research Centre of Finland

mmoralis@csd.auth.gr

Abstract: We demonstrate an optical buffer and a time-slot-interchanger utilizing Si-based spiral delay lines integrated on a micro-scale SOI platform and providing variable delays ranging between 6.5ns and 17.2ns. 10Gbps error-free operation is reported.

OCIS codes: (060.1810) Buffers, couplers, routers, switches, and multiplexers; (230.3120) Integrated optics devices

1. Introduction

One of the key building blocks of next generation optical packet flow networks [1] are Time Slot Interchangers (TSI), allowing programmable time-slot rearrangement of optical packets to reduce contention and provide quality of service (QoS) features. Optical TSI designs, have been extensively studied in the past [2] revealing significant advantages in optical networks, while they have already been demonstrated in different technology implementations utilizing optical switches and fiber-based delay lines [3-5]. Incorporating, however, these functionalities in a photonic router requires a technology platform that would allow for the deployment of both the switching elements and the required delay line stages as integrated structures, enabling ultra-compact and highly-functional TSI configurations suitable for cooperation with integrated switch matrix designs.

Integrated delay lines have been demonstrated via several alternative integration platforms, exploiting asymmetrical MZIs [6], ring resonators [7], Silica on Silicon integration [8-9], thermo-optics switches on Si₃N₄ platform [10], polymer waveguides [11] and the InP platform [12]. Nevertheless, most of these demonstrations offer tunable delay in the range of a few hundred ps [6,7,11], limiting their functionality in terms of packet re-arrangement. Larger delays in the order of >10nsecs have been shown only with SiN-based or Silica-on-Silicon spiral delay lines, yielding, however, a rather low delay efficiency with respect to the required footprint due to the rather moderate refractive index difference of the waveguide platform [8-10]. Recently, integrated waveguide delay lines have been demonstrated on the µm-scale Silicon Photonic (SiPho) platform offering record-low footprint for delay values up to 17.2nsec [13]. The same technology platform has been shown in the past to accommodate also integrated SOA-MZI optical switches [14], so that the combined use of the switches and the integrated delay line structures can form the necessary toolkit for Si-based TSI functionality.

In this paper, we present a variable optical buffer and a TSI layout utilizing a set of three on-chip µm Si-based integrated delay lines with delay values between 6.5ns and 17.2ns, and two differentially-biased SOA-MZI based wavelength converters [15]. The variable optical buffer relies on the use of two WC’s and a delay-line-based stage realized by three integrated Si-based waveguides of different length, while TSI functionality exploits again the two WC’s and a delay-stage that comprises two fiber-based delay lines and an integrated 17.2nsec-inducing Si-spiral. Error-free operation for both the variable optical buffer and the TSI is demonstrated with 10Gb/s NRZ data packets, revealing power penalty, depending on the integrated delay line used, from 3dB to 5dB. The demonstrated optical delay line-based buffering and TSI configurations report the highest delay efficiency values with respect to required footprint of the delay lines, offering a delay efficiency of 2.6ns/mm² that is two orders of magnitude higher than in respective demonstrations so far [7-12] with the highest delay being 17.2ns.

2. Optical Buffer with integrated delay lines

A close-up view of the SiPho chip utilized is shown in Fig.1 (a). The chip is fabricated on VTT’s micro scale silicon photonic platform and comprises three spiral waveguides with lengths of 0.52m, 0.94m and 1.44m, denoted as Delay 1, Delay 2 and Delay 3, respectively. At the sides of each waveguide a taper is used to couple light in and out of the chip, with a total coupling loss of 10dB. An total insertion loss of 20dB, 25dB and 30 dB, including the coupling loss, and an induced delay of 6.5ns, 11.3ns and 17.2nsec are reported for the three waveguides, respectively.
The experimental setup of the variable optical buffer is illustrated in Fig.1(b) It comprises two cascaded wavelength conversion (WC1 and WC2) stages interconnected with an intermediate delay stage. A 1550nm laser beam is modulated in a LiNbO3 modulator, driven by a Programmable Pattern Generator (PPG), to produce a periodic signal with a 256-bit period that incorporates three 35-bit-long 10Gbps NRZ data packets. Every packet consists of a 31-bit payload and a 4-bit header, while a 12-bit long guard band is used between consecutive packets. Packets are split into two identical signals and are injected as control signals into the D and E ports of WC1. Three laser beams ($\lambda_1=1556.55$nm, $\lambda_2=1558.13$nm, $\lambda_3=1559.75$nm) are fed in separate LiNbO3 modulators and driven by respective PPGs to realize 54-bit-long envelope signals at a 40MHz frequency, which are multiplexed in an Arrayed Waveguide Grating (AWG) and are launched into port G of WC1, as the WC1 input signal, after being properly synchronized. The WC1 output signal is injected into the delay stage, which comprises an AWG demultiplexer, the integrated delay lines and an AWG multiplexer. Each integrated delay line is preceded by a CW-powered SOA for compensating the delay line losses. The delay stage output is amplified in an Erbium Doped Fiber Amplifier (EDFA) and is then filtered in a 5nm Optical Band Pass Filter (OBPF) prior being split in two versions that are inserted as the two control signals into WC2. The WC2 input signal was provided by a CW 1550nm laser, after being modulated in a LiNbO3 modulator driven by a PPG to generate again a 50-bit-long optical envelope at a 40 MHz frequency. Both WC1 and WC2 relied on differentially-biased SOA-MZI configurations [15], with WC1 being responsible for deciding upon the appropriate packet delay value and WC2 converting the delayed packets back to their initial wavelength and logic.

As the fiber i/o pitch did not allow for simultaneous fiber-array-based utilization of all three integrated delay lines, the three delays were tested separately by inserting the proper integrated delay into the correct Delay Stage branch. Fig. 2(a) illustrates the initial trace of the three data packets and the corresponding eye diagram of packet (I). Fig. 2(b), (c) and (d) depict packet (I), along with the corresponding eye diagram as it emerges at the WC2 output and after having been delayed in Delay 1, Delay 2 and Delay 3, respectively, through the corresponding integrated delay. An average extinction ratio of 6.5dB was obtained at all three output eye diagrams. Fig. 2(e) depicts the Bit error-rate measurements (BER) revealing error-free operation at a power penalty of less than 3dB for Delays 1 and 2 and less than 5dB for Delay 3. The increased power penalty for Delay3 stems from higher insertion losses of the longer Si-waveguide that yield to higher noise values at the EDFA.

The operational conditions of the optical TSI were as follows: Both SOAs of WC1 were driven at 300mA dc current values, while the optical power of the CW biasing beam was 3.3dBm. The envelope input signal had a peak power of 4.7dBm, while the two control signals entering through port D and E had a peak power of 0.6dBm and 2.4dBm, respectively. In WC2, SOA1 and SOA2 were driven at 260mA and 280mA, respectively, the optical biasing beam was 3dBm, the envelope signal input had a -8dBm peak power value, and the two control signals at ports H and A had peak powers of -3dBm and -6dBm, respectively.

3. Time Slot Interchanger with integrated delay line
The experimental setup for the TSI is illustrated in Fig. 3. The setup shares the main building blocks of the variable optical buffer, along with almost identical operating conditions, differentiating in the delay stage, that in this case comprises two fiber delay lines and one realized with the longest integrated Si-spiral. By synchronizing the three WC1 incoming optical envelopes to have the $\lambda_1$ envelope preceding the $\lambda_3$ envelope, with the $\lambda_2$ envelope being the last envelope in the row, a successful TSI operation can be obtained, as shown in Fig. 4. Fig 4 (a) and (b) depict the traces of the three packets before entering WC1 and before entering WC2, respectively, revealing successful TSI operation.

The output traces of each packet at the WC2 output are shown in Fig. 4(c), (d) and (e), with their corresponding zoom-in versions illustrated in Fig. 4(f), (g) and (h). Finally, the BER measurements and the eye diagrams are shown in Fig. 4 (i), revealing a power-penalty of 3dB for packets II, III and 5dB for packet I that is delayed through the Si-based spiral waveguide.

4. Conclusion

We have presented a variable optical buffer and an optical TSI for 10Gb/s data packets utilizing integrated Si-based waveguide delay lines with a record low footprint of 13.2mm$^2$ and a record high delay efficiency of 2.6nsec/mm$^2$. Given the feasibility of integrating both the SOA-MZI switches and the integrated delay lines on the same $\mu$m SOI platform, the demonstrated buffering and TSI configurations can be in principle implemented as integrated designs that could be utilized in large scale photonic switches architectures.

Acknowledgments

This work has been supported by ICT-STREAMS (Contract No 688172) and ICT-L3MATRIX (Contract No 688544).

References