Optical Interconnect and Memory Components for Disaggregated Computing

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ABSTRACT

High-performance server boards rely on multisocket architectures for increasing the processing power density on the board level and for flattening the data center networks beyond leaf-spine architectures. Scaling, however, the number of processors per board and retaining at the same time low-latency and high-throughput metrics puts current electronic technologies into challenge. In this article, we report on our recent work carried out in the H2020 projects ICT-STREAMS and dREDBox that promotes the use of Silicon Photonic transceiver and routing modules in a powerful board-level, chip-to-chip interconnect paradigm. The proposed on-board platform leverages WDM parallel transmission with a powerful wavelength routing approach that is capable of interconnecting multiple processors with up to 25.6 Tbps on-board throughput, providing direct and collision-less any-to-any communication between multiple compute and memory sockets at low-energy 50 Gbps OOK line-rates. We demonstrate recent advances on the Si-based WDM transceiver, cyclic AWGR router and polymer-based electro-optical circuit board key-enabling technologies, discussing also potential applications in disaggregated rack-scale architectures. We also demonstrate our recent research on optical RAM technologies and optical cache memory architectures that can take advantage of the on-board interconnect technology for yielding true disintegrated computing resolving both power and memory bandwidth bottlenecks of current computational settings.