Board-level Transceiver and Routing technologies for chip-to-chip optical interconnect architectures

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Abstract—We present the ICT-STREAMS optical interconnect architecture and report on the recent advancements of its O-band silicon photonic key building-blocks namely a 4x40Gbps transmitter and an 8x8 Arrayed Waveguide Grating Router (AWGR) device.

Keywords—Optical interconnect, silicon photonics, wavelength routing, wavelength division multiplexing, optical transceiver

I. INTRODUCTION

The explosive growth of intra-Data Center (DC) traffic generated by data-intensive cloud applications and Big Data-driven computational machines, is currently stretching the limits of the DC infrastructure, calling for both interconnect and computational advancements [1]. This ambitious target cannot anymore rely on simply scaling the number of cores in the microprocessors, since this approach is already facing practical real-estate limitations and cost scaling problems [2]. As such, research focus has now shifted to chip-to-chip communication solutions for multi-core server-boards (MSBs), exploiting the physical proximity of the processors in order to enable faster and energy-efficient links between sockets while achieving low cost. Today, MSBs such as Intel’s QuickPath Interconnect (QPI) [3] are limited to host only up to 4 point-to-point (p2p) directly interconnected sockets and scaling beyond 4-socket configurations relies on indirect connections among 4-socket clusters. On top of this, 65% of the QPI links bandwidth is wasted for cache coherence updates. As such, active switches, such as PCIe or Bixby switches[4] are usually employed for more than 4-socket configurations as they can deliver unlimited connectivity, but this benefit comes with the cost of increased energy consumption and latency.

In this context, on-board optical interconnection has recently emerged as an attractive solution to satisfy the high bandwidth demands and enable direct interconnection beyond 4-sockets [5]. So far, AWGR-based interconnects have been proposed delivering important advantages when used in MSBs demonstrating 10 Gb/s data rates [6],[7] with network simulations for different workloads demonstrated 3× energy savings compared to the respective electronic MSB baseline [6]. Still, the proposed scheme is restricted to the C-band region and to 10 Gb/s line-rates [6], while proof-of-concept demonstration using C-band integrated photonic circuitry have been experimentally shown as Network-on-Chip (NoC) layouts without exceeding 0.3 Gb/s data-rate performance [8] limiting its applicability in NoC systems such as high-speed MSB architectures. Meanwhile, the well-established short-reach O-band interconnect infrastructure remains unexploited although it appears as an attractive spectral region due to the low-loss waveguide features it can offer.

In this paper, we present the ICT-STREAMS project’s [9] optical interconnect architectural concept that uses O-band silicon photonic WDM-enabled transceivers and an AWGR to achieve high-bandwidth and energy-efficient any-to-any communication among sockets in an MSB environment. We also report on the latest achievements of O-band silicon photonics key building-blocks of this architecture i.e. a WDM 4×40Gb/s transmitter and a compact, low-loss 8x8 AWGR.

II. ICT-STREAMS AWGR-BASED INTERCONNECT ARCHITECTURE

Fig. 1 presents the ICT-STREAMS optical interconnect architecture in a generic N-socket layout, where an all-passive silicon photonic NxN AWGR routing element provides single-hop any-to-any communication among N processor sockets. Each socket is electrically connected to a WDM-enabled Tx optical engine equipped with N-1 laser diodes (LD), each one operating at a different wavelength. Every LD feeds a different RM to imprint the electrical data sent from the socket to each one of the N-1 wavelengths, so that the Tx engine comprises N-1 RMs along with their respective RM drivers (DR). All RMs are implemented on the same optical bus to produce the WDM-encoded data stream of each socket. The data stream generated by each socket enters the input port of the AWGR and gets routed through the AWGR to a destination output based on its cyclic-frequency routing properties. In this way, every socket can forward data to any of the remaining 7 sockets by simply modulating its electrical data onto a different wavelength via the respective RM, allowing direct single-hop communication between all sockets through a passive wavelength-routing.

![Fig. 1. Proposed optical NxN AWGR-based interconnection concept for MSB connectivity exploiting WDM-enabled Tx/Rx engines.](image-url)
At every Rx engine, the received WDM-encoded data stream gets demultiplexed with a 1:(N-1) optical demultiplexer (DEMUX), so that every wavelength is received by a distinct PD. Each PD is then connected to a TIA that provides the socket with the respective electrical signal.

III. SILICON PHOTONIC TRANSCiever & ROUTer AND EXPERIMENTAL RESULTS

Within the ICT-STREAMS project an O-band silicon photonic compact 8x8 AWGR device [10] and a 4-channel WDM-enabled silicon photonic transceiver [11] have been developed. A microscope image of the fabricated AWGR is shown in Fig.2a). The AWGR was designed at a center wavelength of 1301 nm, targeting a channel spacing equal to 10 nm, a 3-dB bandwidth of 5.7nm, an FSR of 80 nm and Passband Peak Deviation (PPD) of below 6 nm. The fabrication of the integrated AWGR relied on the imec-ePIXfab silicon photonics passesive technology using a 220 nm-thick Si and 2 μm-thick buried oxide layer. The device also exhibits a footprint of 700x270 μm². The static device characterization revealed a 11dB channel crosstalk, 3.5dB loss non-uniformity and 2.5dB best case insertion losses. The spectral response of all port combinations of the AWGR is shown in Fig.2b) indicating proper cyclic-frequency operation that can be verified by the same-colored output responses for each one of the different input ports.

The 4-channel WDM transmitter relies on micro-ring resonators featuring 4x40 Gb/s data generation operation and an energy efficiency of 24.84 fJ/bit/RM under 1.82 Vpp drive. It was fabricated via a custom run within IMEC’s ISISP50G silicon photonics technological platform. A microscope photo of the fabricated chip is depicted in 3a). The transmitter consists of an array of 4 high-speed carrier-depletion micro-ring modulators with 7.5 μm, 7.502 μm, 7.504 μm and 7.506 μm radius and ~8.9 nm (1.58 THz) resonance wavelength spacing, corresponding to RMS of Tx channels 1-4, respectively. The chip comprises also a 4-channel receiver (Rx) part that can be accessed through the Rx in input port. Fig. 3b-d) illustrates the eye diagrams of the generated NRZ signals at 40 Gb/s as obtained at Tx output for every wavelength channel separately, exhibiting ER values of 4.4 dB, 4.1 dB, 4.2 dB and 4 dB, respectively. The RMSs were driven with a peak-to-peak voltage of 1.78 Vpp, 1.8 Vpp, 1.85 Vpp and 1.85 Vpp, respectively, while the applied DC bias reverse voltages were 3.17 V, 2.8 V, 2.82 V and 2.85 V, respectively. The average optical power of the signal at the four wavelengths (0.1-0.4) before entering the transmitter chip was 10 dBm, while the average power of the modulated signals at the four wavelengths emerging at the output of the chip were measured to be -17.8 dBm, -18.2 dBm, -17.7 dBm and -15.7 dBm, respectively.

IV. CONCLUSION

We report on our recent results of the ICT-STREAMS energy-efficient optical interconnect architecture.

V. ACKNOWLEDGMENTS

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